1. OVERVIEW

The μPD720210 is a USB 3.0 hub controller that complies with the Universal Serial Bus (USB) Specification Revision 3.0 and operates at up to 5 Gbps. The device incorporates Renesas' market proven design expertise in USB 3.0 interface technologies and market proven USB 2.0 hub core. The device is fully compatible with all prior versions of USB and 100% compatible with Renesas' industry standard USB 3.0 host controller. It comes in a small 76-pin QFN package and integrates several commonly required external components, making it ideally suited for applications with limited PCB space. In addition, the μPD720210 incorporates Renesas' low-power technologies.

1.1 Features

- Compliant with Universal Serial Bus 3.0 Specification Revision 1.0, which is released by USB Implementers Forum, Inc
  - Supports the following speed data rate as follows: Low-speed (1.5Mbps) / Full-speed (12Mbps) / High-speed (480Mbps) / Super-speed (5Gbps)
  - Supports USB3.0 link power management (U0/U1/U2/U3)
  - Supports USB2.0 link power management (LPM: L0/L1/L2/L3)
- Configurable downstream port number of 2/3/4
- Supports all VBUS control
  - Individual or Global over-current detection
  - Individual or Ganged power control
- Supports downstream port status with LED
- Supports USB3.0/2.0 Compound (non-removable) devices by I/O pin configuration
- Supports clock output (24/12MHz) for Compound (non-removal) device on downstream ports
- Support Energy Star for PC peripheral system
- Single 5V Power Supply
  - On chip LDO for 3.3v from 5v input and Switching Regulator for 1.05v from 5v input (TBD)
- System clock: 24 MHz Crystal or Oscillator
- Supports USB Battery Charging Specification Revision 1.2 and other portable devices
  - DCP mode of BC 1.2
  - CDP mode of BC 1.2
  - China Mobile Phone Chargers
  - EU Mobile Phone Chargers
  - Blackberry, Apple
- Supports Optional SPI ROM
  - Vendor ID / Product ID / UUID
- Small Footprint
  - Small and low pin count package with simple pin assignment for PCB layout
  - Integration of many peripheral components
  - Direct routing of all USB signal traces to connector pins only on the top layer
- Automatic switching between Self/Bus-Powered modes
- Integrated Termination resistors for USB
- Fine PHY Controls for Certification
  - Pre-emphasis Control (USB3.0)
  - Amplitude Adjustment (USB2.0/3.0)
- Provides SUSPEND Status output

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1.2 Applications

Stand-alone Hub, Monitor-Hub, Docking Station, Integrated Hub, etc.

1.3 Ordering Information

Part Number	Package	Remark
μPD720210K8-BAF-A	76-pin QFN (9 × 9)	Lead-free product

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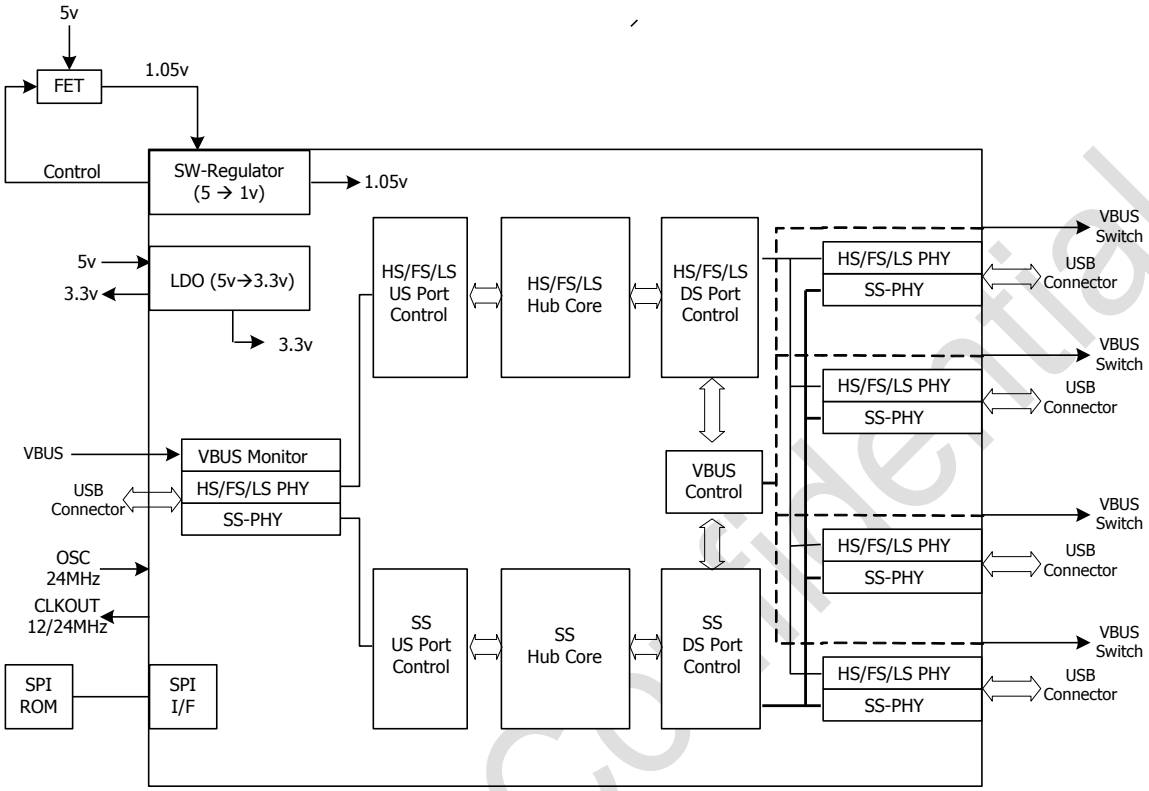
1.4 Block Diagram

Figure 1-1 μPD720210 Block Diagram



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Block Name	Description
SS PHY	For super-speed Tx/Rx
HS/FS/LS PHY	For high-/full-/low-speed Tx/Rx
Port Power CTL	The port power (VBUS) on/off control for each port.
VBUS Monitor	This block monitors the VBUS level of the upstream port.
SS US Port Control	Upstream port control logic for SuperSpeed
HS/FS/LS US Port Control	Upstream port control logic for high-/full-/low-speed
SS Hub Core	The central control logic for this SS-Hub system.
HS/FS/LS Hub Core	The central control logic for this HS/FS/LS Hub system.
SS DS Port Control	Downstream port control logic for SuperSpeed
HS/FS/LS DS Port Control	Downstream port control logic for HS/FS/LS
VBUS Control	This block has the top layer of the control of all the port power switches according to the setting.
SPI Interface	Connected to external serial ROM which can hold the optional firmware and hub settings
SW-Regulator	Switching regulator control logic to output 1.05v power from 5v input, utilizing the external transistor
LDO	Low DropOut regulator integrated in this hub

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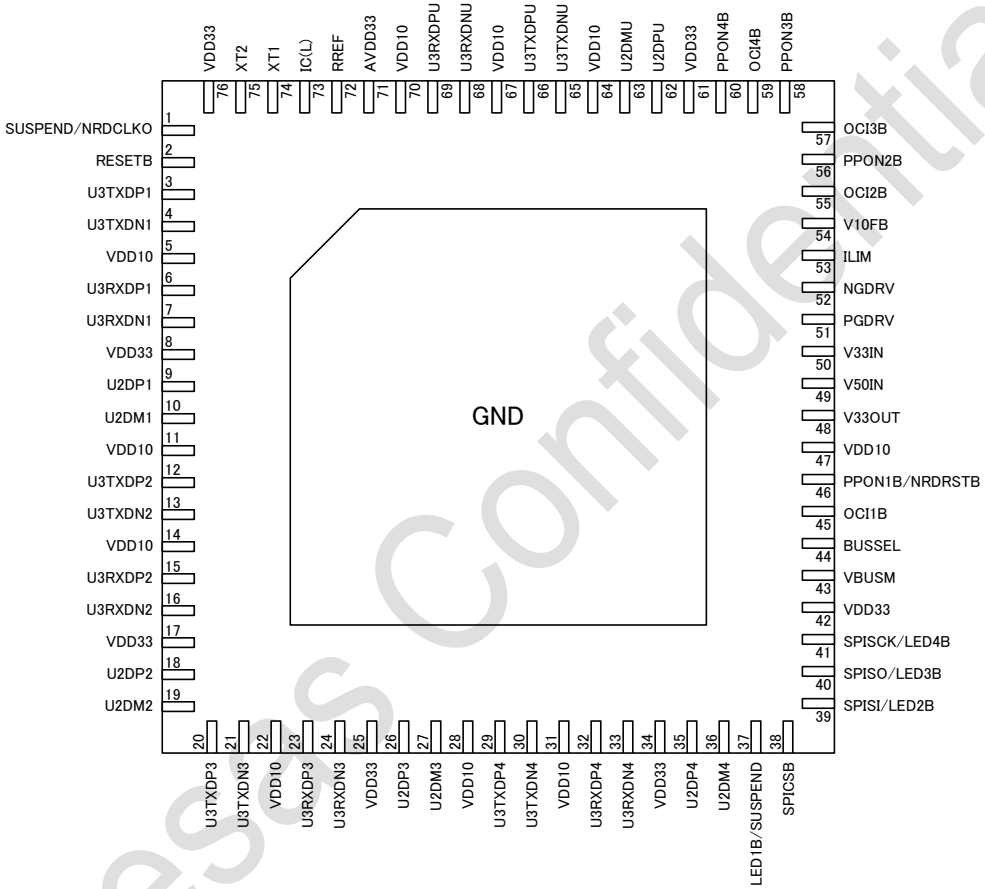
1.5 Pin Configuration

- **76-pin QFN (9 × 9)**
  μPD720210K8-BAF-A

Figure 1-2 Pin Configuration of μPD720210 (Top View)



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2. PIN FUNCTION

This section describes each pin functions.

Strapping Option column in the tables shows the pin can be used to configure the functional settings of this controller when it is pulled up/down. See the related chapter number shown in the column for detail.

2.1 Power supply

Pin Name	Pin No.	I/O Type	Function
VDD10	5, 11, 14, 22, 28, 31, 47, 64, 67, 70	Power	1.05V power supply for Core Logic
VDD33	8, 17, 25, 34, 42, 61, 76	Power	3.3V power supply for IO buffer
AVDD33	71	Power	3.3V power supply forAnalog circuit
V50IN	49	Power	LDO/SW Regulator 5V Input
V33OUT	48	Power	LDO 3.3V Output
V33IN	50	Power	SW Regulator 3.3V Input
NGDRV	52	-	SW Regulator Nch FET Control
PGDRV	51	-	SW Regulator Pch FET Control
ILIM	53	-	SW Regulator Current Sense
V10FB	54	-	SW Regulator Output Monitor

2.2 Analog Interface

Pin Name	Pin No.	I/O Type	Function
RREF	72	-	Reference Voltage Input for USB2.0 RREF must be connected 1% accuracy of reference resistor of 1.6kΩ .

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2.3 System Clock

Pin Name	Pin No.	I/O Type	Function
XT1	74	IN	External Oscillator Input Connect to 24MHz crystal or 3V Oscillator input
XT2	75	OUT	External Oscillator Output Connect to 24MHz crystal In using single-ended clock input to XT1, this pin should be left open.

2.4 System Interface Pins

Pin Name	Pin No.	I/O Type	Active Level	Function
SUSPEND/NRDCLKO	1	OUT	High/NA	SUSPEND Output or CLKOUT
VBUSM	43	IN	High	Upstream Port VBUS Monitor
BUSSEL	44	IN	N/A	Power Mode Select Input 0: Bus-power setting 1: Self-power setting
LED1B/SUSPEND	37	OUT	Low	LED for port1 or SUSPEND Output, depending on pin strap setting of SPICSB. LED for port2 to 4 is described in 2.7.
RESETB	2	IN	Low	Chip Reset Input

2.5 USB Port Control Pins

Pin Name	Pin No.	I/O Type	Active Level	Function
OCI1B, OCI2B, OCI3B, OCI4B	45, 55, 57, 59	IN	Low	Over Current Input 0: Over-current condition is detected. 1: Non over-current condition is detected. These pins are used for pin strapping option to set non-removal setting.
PPON1B/NRDRSTB, PPON2B, PPON3B, PPON4B	46, 56, 58, 60	I/O	Low	Port Power Control 0: Power supply for Vbus is on. 1: Power supply for Vbus is off. These pins are used for pin strapping option. PPON4B, PPON3B: Number of Ports PPON2B: Gang/Individual Power Control PPON1B: Clock output enable for on-board Compound (non-removable) Device See μPD720210 User's Manual for detail.

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2.6 USB Data Pins

Pin Name	Pin No.	I/O Type	Function
U3TXDN1, U3TXDN2, U3TXDN3, U3TXDN4	4, 13, 21, 30	OUT	USB3.0 Downstream Transmit data D- signal for super-speed
U3TXDNU	65	OUT	USB3.0 Upstream Transmit data D- signal for super-speed
U3TXDP1, U3TXDP2, U3TXDP3, U3TXDP4	3, 12, 20, 29	OUT	USB3.0 Downstream Transmit data D+ signal for super-speed
U3TXDPU	66	OUT	USB3.0 Upstream Transmit data D+ signal for super-speed
U3RXDN1, U3RXDN2, U3RXDN3, U3RXDN4	7, 16, 24, 33	IN	USB3.0 Downstream Receive data D- signal for super-speed
U3RXDNU	68	OUT	USB3.0 Upstream Receive data D- signal for super-speed
U3RXDP1, U3RXDP2, U3RXDP3, U3RXDP4	6, 15, 23, 32	IN	USB3.0 Downstream Receive data D+ signal for super-speed
U3RXDPU	69	OUT	USB3.0 Upstream Receive data D+ signal for super-speed
U2DM1, U2DM2, U2DM3, U2DM4	10, 19, 27, 36	I/O	USB2.0 Downstream D- signal for high-/full-/low-speed
U2DMU	63	I/O	USB2.0 Upstream D- signal for high-/full-/low-speed
U2DP1, U2DP2, U2DP3, U2DP4	9, 18, 26, 35	I/O	USB2.0 Downstream D+ signal for high-/full-/low-speed
U2DPU	62	I/O	USB2.0 Upstream D+ signal for high-/full-/low-speed

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2.7 SPI Interface

Pin Name	Pin No.	I/O Type	Active Level	Function
SPISCK/LED4B	41	OUT	N/A	External serial ROM Clock Output
SPICSB	38	OUT	Low	External serial ROM Chip Select This pin is used for pin strap option to select external ROM or LED.
SPISO/LED3B	40	I/O	N/A	External serial ROM Data Input (to be connected to Serial Data Output pin of the external ROM) or LED output, depending on pin strap setting of SPICSB.
SPISI/LED2B	39	OUT	N/A	External serial ROM Data Output (to be connected to Serial Data input pin of the external ROM) or LED output, depending on pin strap setting of SPICSB.

2.8 Test Pin

Pin Name	Pin No.	I/O Type	Active Level	Function
IC(L)	73	IN	High	Test Pin to be connected to GND

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3. ELECTRICAL SPECIFICATIONS

3.1 Buffer List

- 3.3 V input buffer

  IC(L)
- 3.3 V input Schmidt buffer

  RESETB, OCI2B, OCI3B, OCI4B
- 3.3 V I_{OLH} = 4mA output buffer

  SUSPEND/NRDCLKO, SPICSB, PPON1B/NRDRSTB, PPON2B, PPON3B, PPON4B
- 3.3 V I_{OLH} = 12mA output buffer

  LED1B/SUSPEND, SPISO/LED2B, SPISCK/LED4B
- 3.3 V I_{OL} = 12mA bi-directional buffer

  SPISI/LED3B,
- 5 V input Schmidt buffer

  VBUSM, BUSSEL, OCI1B
- • 3.3 V oscillator interface

  XT1, XT2
- USB Classic interface

  U2DP(4:1, U), U2DM(4:1, U), RREF
- USB Super-speed Serdes (Serializer-Deserializer)

  U3TXDP(4:1, U), U3TXDN(4:1, U), U3RXDP(4:1, U), U3RXDN(4:1, U)
- LDO Interface

  V33OUT, V50IN
- Switching Regulator Interface

  V33IN, PGDRV, NGDRV, ILIM, V10FB

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3.2 Terminology

Table 3-1 Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD10}, AV_{DD33}	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a VDD pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into output pin.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is applied to the device.

Table 3-2 Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD10}, AV_{DD33}	Indicates the voltage range for normal logic operations occur when GND = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “Max.” value is applied, the input voltage is guaranteed as low level voltage.
Input rise time	T_{ri}	Indicates the limit value for the time period when an input voltage applied to the input pins of the device rises from 10% to 90%.
Input fall time	T_{fi}	Indicates the limit value for the time period when an input voltage applied to the input pins of the device falls from 90% to 10%.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.

Table 3-3 Term Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.

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3.3 Absolute Maximum Ratings

Table 3-4 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Units
Power supply voltage	V_{DD33}, AV_{DD33}		−0.5 to +4.6	V
	V_{DD10}		−0.5 to +1.4	V
	V50IN		TBD	V
Input voltage, 3.3 V buffer	V_I	$V_I < V_{DD33}$ + 0.5 V	−0.5 to +4.6	V
Output voltage, 3.3 V buffer	V_O	$V_O < V_{DD33}$ + 0.5 V	−0.5 to +4.6	V
Input voltage, 5 V buffer	V_I	$V_I < V_{DD33}$ + 2.5 V	−0.5 to +6.6	V
Output current	I_O	4 mA Type	8	mA
	I_O	12mA Type	24	mA
Storage temperature	T_{stg}		−65 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

3.4 Recommended Operating Ranges

Table 3-5 Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating voltage	V_{DD33}, AV_{DD33}		3.0	3.3	3.6	V
	V_{DD10}		0.9975	1.05	1.1025	V
High-level input voltage	V_{IH}		2.0		V_{DD33}+0.3	V
Low-level input voltage	V_{IL}		−0.3		0.8	V
Input rise time	T_{ri}	Normal Buffer	0		200	ns
		Schmitt Buffer	0		10	ms
Input fall time	T_{fi}	Normal Buffer	0		200	ns
		Schmitt Buffer	0		10	ms
Operating ambient temperature	T_A		0		+70	°C

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3.5 DC Characteristics

Table 3-6 DC Characteristics (V_{DD33} = 3.3 V ± 10%, V_{DD10} = 1.05 V ± 5%, T_A = –0 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Units
Off-state output current	I_{OZ}	VI = V_{DD33} or GND		±10	μA
Input leakage current	I_I	VI = V_{DD33} or GND		±10	μA
Low-level output voltage	V_{OL}	IOL = 0mA		0.1	V
High-level output voltage	V_{OH}	IOH = 0mA	V_{DD33}-0.1		V

Table 3-7 USB interface block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Output pin impedance	Z_{HSDRV}		40.5	49.5	Ω
Input Levels for Low-/full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	V
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	|(D+) – (D–)|	0.2		V
Differential common mode range	V_{CM}	Includes VDI range	0.8	2.5	V
Output Levels for Low-/full-speed:					
High-level output voltage	V_{OH}	RL of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V_{OL}	RL of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		–50	+500	mV
High-speed differential input signaling level	See Figure 4-4				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		–10	+10	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		–10	+10	mV
Chirp J level (differential signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (differential signal)	V_{CHIRPK}		–900	–500	mV

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Figure 3-1. Differential Input Sensitivity Range for Low-/full-speed

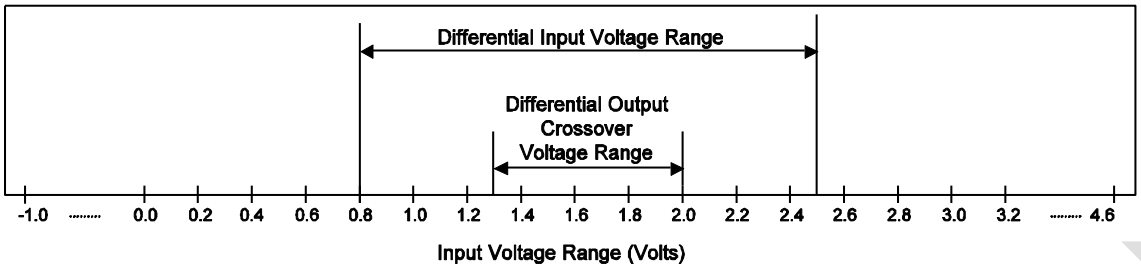

Figure 3-2. Full-speed Buffer VOH/IOH Characteristics for High-speed Capable Transceiver

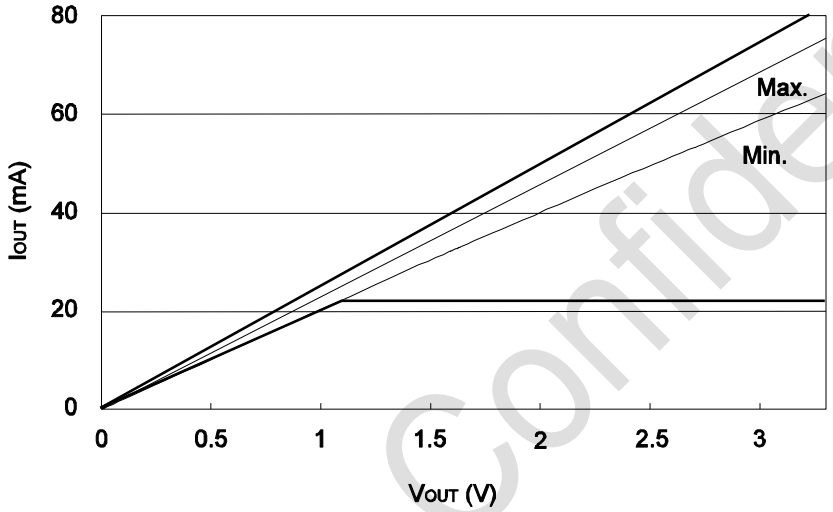

Figure 3-3. Full-speed Buffer VOL/IOL Characteristics for High-speed Capable Transceiver

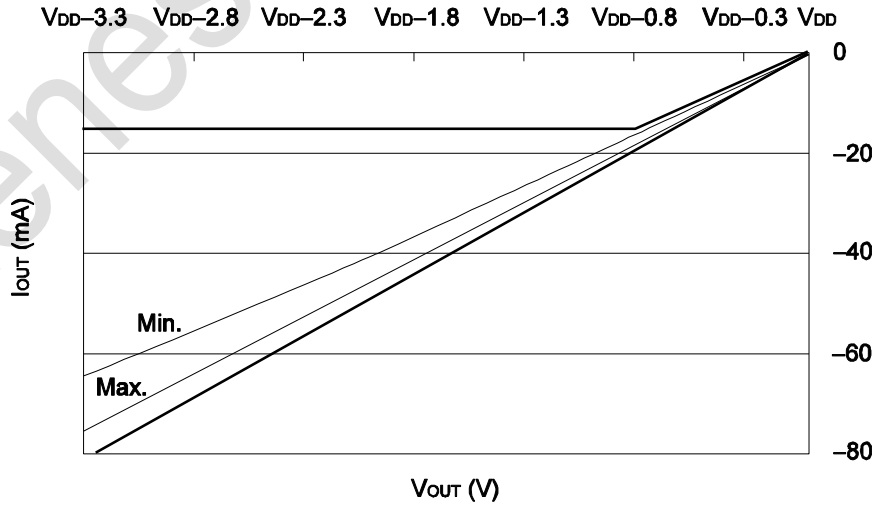

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Figure 3-4. Receiver Sensitivity for Transceiver at DP/DM

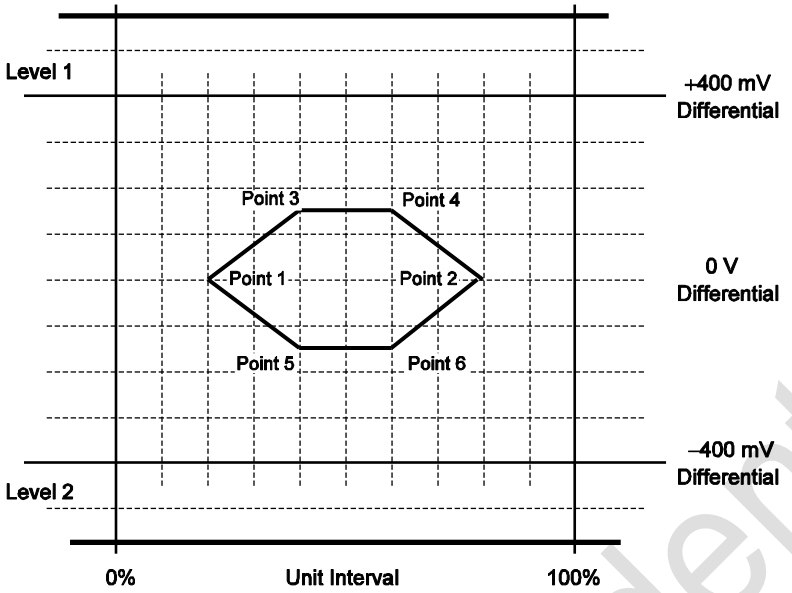
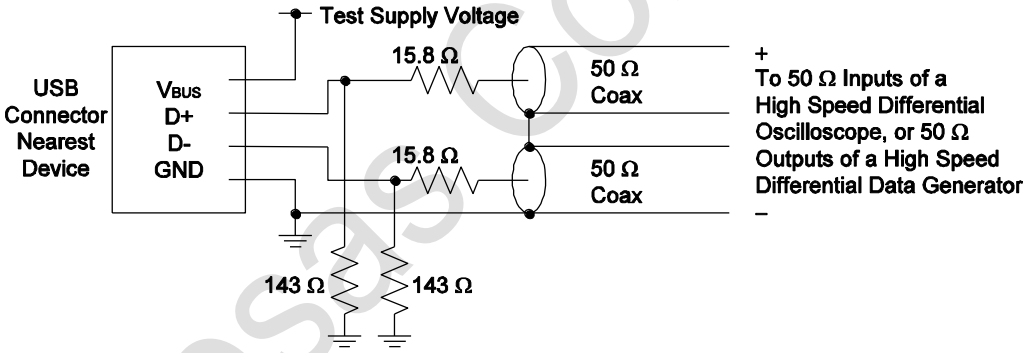


Figure 3-5. Receiver Measurement Fixtures



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3.6 Pin Capacitance

Table 3-8 Pin capacitance

Parameter	Symbol	Condition	Min.	Max.	Units
SPI Interface Pin capacitance	C_{SPI}			5	pF

3.7 Sequence for turning on or off power: TBD

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3.8 AC Characteristics

3.8.1 System Clock

Table 3-9 System clock (XT1/XT2) ratings (V_{DD33} = 3.3 V ± 10%, V_{DD10} = 1.05 V ± 5%, T_A = –0 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Clock frequency	F_{CLK}	Crystal	–100 ppm	24	+100 ppm	MHz
Clock duty cycle	T_{DUTY}		40	50	60	%

Remark Required accuracy of crystal or oscillator block includes initial frequency accuracy, the spread of Crystal capacitor loading, supply voltage, temperature and aging, etc.

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3.8.2 Reset

Reset and Clock Timing: TBD

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3.8.3 USB3.0 SuperSpeed Interface – Differential Transmitter (TX) Specifications

(Refer to Universal Serial Bus 3.0 Specification Revision 1.0 for more information)

Table 3-10 Transmitter Normative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Unit Interval	UI	199.94	200.06	ps
Differential p-p Tx voltage swing	$V_{TX-DIFF-PP}$	0.8	1.2	V
Tx de-emphasis	$V_{TX-DE-RATIO}$	3.0	4.0	dB
DC differential impedance	$R_{TX-DIFF-DC}$	72	120	Ω
The amount of voltage change allowed during Receiver Detection	$V_{TX-RCV-DETECT}$		0.6	V
AC Coupling Capacitor	$C_{AC-COUPLING}$	75	200	nF
Maximum slew rate	$t_{CDR-SLEW-MAX}$		10	ms/s

Table 3-11 Transmitter Informative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Deterministic min pulse	$t_{MIN-PULSE-Dj}$	0.96		UI
Tx min pulse	$t_{MIN-PULSE-Tj}$	0.90		UI
Transmitter Eye	t_{TX-EYE}	0.625		UI
Tx deterministic jitter	$t_{TX-DJ-DD}$		0.205	UI
Tx input capacitance for return loss	$C_{TX-PARASITIC}$		1.25	pf
Transmitter DC common mode impedance	R_{TX-DC}	18	30	Ω
Transmitter short-circuit current limit	$I_{TX-SHORT}$		60	mA
Transmitter DC common-mode voltage	$V_{TX-DC-CM}$	0	2.2	V
Tx AC common mode voltage	$V_{TX-CM-AC-PP-ACTIVE}$		100	mVp-p
Absolute DC Common Mode Voltage between U1 and U0	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$		200	mV
Electrical Idle Differential Peak- Peak Output voltage	$V_{TX-IDLE-DIFF-AC-pp}$	0	10	mV
DC Electrical Idle Differential Output Voltage	$V_{TX-IDLE-DIFF-DC}$	0	10	mV

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3.8.4 USB3.0 SuperSpeed Interface – Differential Receiver (RX) Specifications

(Refer to Universal Serial Bus 3.0 Specification Revision 1.0 for more information)

Table 3-12 Receiver Normative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Unit Interval	UI	199.94	200.06	ps
Receiver DC common mode impedance	R_{RX-DC}	18	30	Ω
DC differential impedance	$R_{RX-DIFF-DC}$	72	120	Ω
DC Input CM Input Impedance for V>0 during Reset of Power down	$Z_{RX-HIGH-IMP-DC-POS}$	25k		Ω
LFPS Detect Threshold	$V_{RX-LFPS-DET-DIFF-p-p}$	100	300	mV

Table 3-13 Receiver Informative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Differential Rx peak-to-peak voltage	$V_{RX-DIFF-PP-POST-EQ}$	30		mV
Max Rx inherent timing error	T_{RX-Tj}		0.45	UI
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD}$		0.285	UI
Rx input capacitance for return loss	$C_{RX-PARASITIC}$		1.1	pF
Rx AC common mode voltage	$V_{RX-CM-AC-P}$		150	mVPeak
Rx AC common mode voltage during the U1 to U0 transition	$V_{RX-CM-DC-ACTIVE-IDLE-DELTA-P}$		200	mVPeak

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3.8.5 USB2.0 Interface

(1/4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Low-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{LR}	C_L = 200 pF to 600 pF	75	300	ns
Fall time (90% to 10%)	t_{LF}	C_L = 200 pF to 600 pF	75	300	ns
Differential rise and fall time matching	t_{LRFM}	(t_{LR}/t_{LF}) **Note**	80	125	%
Low-speed data rate	$t_{LDRATHS}$	Average bit rate	1.49925	1.50075	Mbps
Downstream facing port source jitter total (including frequency tolerance) (**Figure 3-10**):					
To next transition	t_{DDJ1}		−25	+25	ns
For paired transitions	t_{DDJ2}		−14	+14	ns
Downstream facing port differential receiver jitter total (including frequency tolerance) (**Figure 3-12**):					
To next transition	t_{UJR1}		−152	+152	ns
For paired transitions	t_{UJR2}		−200	+200	ns
Source SE0 interval of EOP (**Figure 3-11**)	t_{LEOPT}		1.25	1.5	μs
Receiver SE0 interval of EOP (**Figure 3-11**)	t_{LEOPR}		670		ns
Width of SE0 interval during differential transition	t_{LST}			210	ns
Hub differential data delay (**Figure 3-8**)	t_{LHDD}			300	ns
Hub differential driver jitter (including cable) (**Figure 3-8**):					
Downstream facing port					
To next transition	t_{LDHJ1}		−45	+45	ns
For paired transitions	t_{LDHJ2}		−15	+15	ns
Upstream facing port					
To next transition	t_{LUHJ1}		−45	+45	ns
For paired transitions	t_{LUHJ2}		−45	+45	ns
Data bit width distortion after SOP (**Figure**)	t_{LSOP}		−60	+60	ns
Hub EOP delay relative to t_{HDD} (**Figure 3-9**)	t_{LEOPD}		0	200	Ns
Hub EOP output width skew (**Figure 3-9**)	t_{LHESK}		−300	+300	Ns
Full-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{FR}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Fall time (90% to 10%)	t_{FF}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms

Note Excluding the first transition from the Idle state.

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Parameter	Symbol	Conditions	Min.	Max.	Unit
Full-speed Electrical Characteristics (Continued)					
Consecutive frame interval jitter	t_{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance) (**Figure0**): To next transition For paired transitions	 t_{DJ1} t_{DJ2}	**Note**	 −3.5 −4.0	 +3.5 +4.0	 ns ns
Source jitter for differential transition to SE0 transition (**Figure3-11**)	t_{FDEOP}		−2	+5	ns
Receiver jitter (**Figure3-12**): To Next Transition For Paired Transitions	 t_{JR1} t_{JR2}		 −18.5 −9	 +18.5 +9	 ns ns
Source SE0 interval of EOP (**Figure3-11**)	t_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP (**Figure3-11**)	t_{FEOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns
Hub differential data delay (**Figure3-8**) (with cable) (without cable)	 t_{HDD1} t_{HDD2}		 	 70 44	 ns ns
Hub differential driver jitter (including cable) (**Figure3-8**): To next transition For paired transitions	 t_{HDJ1} t_{HDJ2}		 −3 −1	 +3 +1	 ns ns
Data bit width distortion after SOP (**Figure3-8**)	t_{FSOP}		−5	+5	ns
Hub EOP delay relative to t_{HDD} (**Figure 3-9**)	t_{FEOPD}		0	15	ns
Hub EOP output width skew (**Figure 3-9**)	t_{FHESK}		−15	+15	ns
High-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{HSR}		500		ps
Fall time (90% to 10%)	t_{HSF}		500		ps
Driver waveform	See **Figure3-7**.				
High-speed data rate	t_{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t_{HSRFI}			4 high-speed	Bit times
Data source jitter	See **Figure3-7**.				
Receiver jitter tolerance	See **Figure** 3-4**3-4**.				
Hub data delay (without cable)	t_{HSHDD}			36 high-speed+4 ns	Bit times
Hub data jitter	See **Figure** 3-4**3-4**, **Figure3-7**.				
Hub delay variation range	t_{HSHDV}			5 high-speed	Bit times

Note Excluding the first transition from the Idle state.

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Parameter	Symbol	Conditions	Min.	Max.	Unit
Hub Event Timings					
Time to detect a downstream facing port connect event (**Figure3-14**): Awake hub Suspended hub	t_{DCNN}		 2.5 2.5	 2000 12000	 μs μs
Time to detect a disconnect event at a hub's downstream facing port (**Figure3-13**)	t_{DDIS}		2.0	2.5	μs
Duration of driving resume to a downstream port (only from a controlling hub)	t_{DRSMDN}		20		ms
Time from detecting downstream resume to rebroadcast	t_{URSM}			1.0	ms
Duration of driving reset to a downstream facing port (**Figure3-15**)	t_{DRST}	Only for a SetPortFeature (PORT_RESET) request	10	20	ms
Time to detect a long K from upstream	t_{URLK}		2.5	100	μs
Time to detect a long SE0 from upstream	t_{URLSE0}		2.5	10000	μs
Duration of repeating SE0 upstream (for low-/full-speed repeater)	t_{URPSE0}			23	FS Bit times
Inter-packet delay (for high-speed) of packets traveling in same direction	$t_{HSIPDSD}$		88		Bit times
Inter-packet delay (for high-speed) of packets traveling in opposite direction	$t_{HSIPDOD}$		8		Bit times
Inter-packet delay for device/root hub response with detachable cable for high-speed	$t_{HSRSPIPD1}$			192	Bit times
Time of which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake	t_{FILT}		2.5		μs
Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence	t_{WTDCH}			100	μs
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset	t_{DCHBIT}		40	60	μs
Time before end of reset by which a hub must end its downstream chirp sequence	t_{DCHSE0}		100	500	μs
Time from internal power good to device pulling D+ beyond V_{IHZ} (**Figure3-15**)	t_{SIGATT}			100	ms
Debounce interval provided by USB system software after attach (**Figure3-15**)	t_{ATTDB}			100	ms
Maximum duration of suspend averaging interval	$t_{SUSAVGI}$			1	s
Period of idle bus before device can initiate resume	t_{WTRSM}		5		ms
Duration of driving resume upstream	t_{DRSMUP}		1	15	ms

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Parameter	Symbol	Conditions	Min.	Max.	Unit
Hub Event Timings (Continued)					
Resume recovery time	t_{RSMRCY}	Remote-wakeup is enabled	10		ms
Time to detect a reset from upstream for non high-speed capable devices	t_{DETRST}		2.5	10000	μs
Reset recovery time (**Figure3-15**)	t_{RSTRCY}			10	ms
Inter-packet delay for full-speed	t_{IPD}		2		Bit times
Inter-packet delay for device response with detachable cable for full-speed	$t_{RSPIPD1}$			6.5	Bit times
SetAddress() completion time	$t_{DSETADDR}$			50	ms
Time to complete standard request with no data	$t_{DRQCMPLTND}$			50	ms
Time to deliver first and subsequent (except last) data for standard request	$t_{DRETDATA1}$			500	ms
Time to deliver last data for standard request	$t_{DRETDATAN}$			50	ms
Time for which a suspended hub will see a continuous SE0 on upstream before beginning the high-speed detection handshake	$t_{FILTSE0}$		2.5		μs
Time a hub operating in non-suspended full-speed will wait after start of SE0 on upstream before beginning the high-speed detection handshake	$t_{WTRSTFS}$		2.5	3000	ms
Time a hub operating in high-speed will wait after start of SE0 on upstream before reverting to full-speed	t_{WTREV}		3.0	3.125	ms
Time a hub will wait after reverting to full-speed before sampling the bus state on upstream and beginning the high-speed will wait after start of SE0 on upstream before reverting to full-speed	$t_{WTRSTHS}$		100	875	ms
Minimum duration of a Chirp K on upstream from a hub within the reset protocol	t_{UCH}		1.0		ms
Time after start of SE0 on upstream by which a hub will complete its Chirp K within the reset protocol	t_{UCHEND}			7.0	ms
Time between detection of downstream chip and entering high-speed state	t_{WTHS}			500	μs
Time after end of upstream Chirp at which hub reverts to full-speed default state if no downstream Chirp is detected	t_{WTFS}		1.0	2.5	ms

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Figure3-6. Transmit Waveform for Transceiver at DP/DM

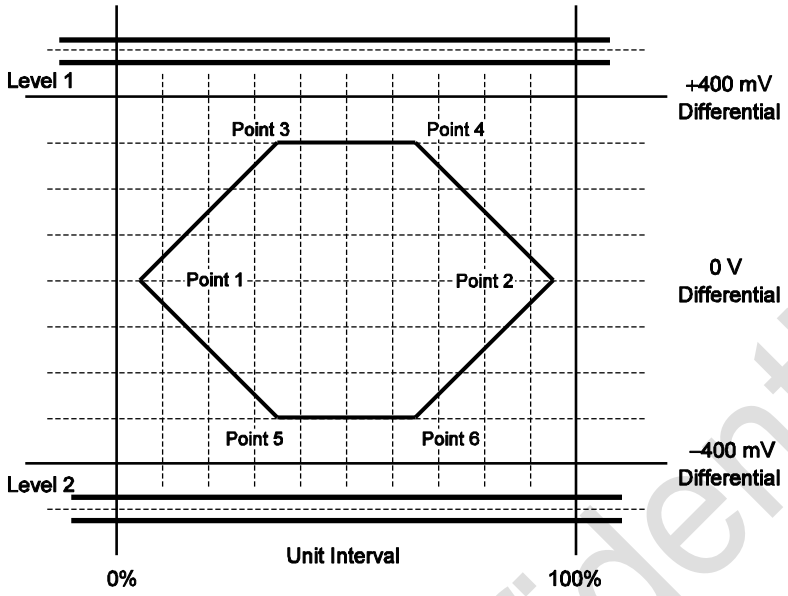
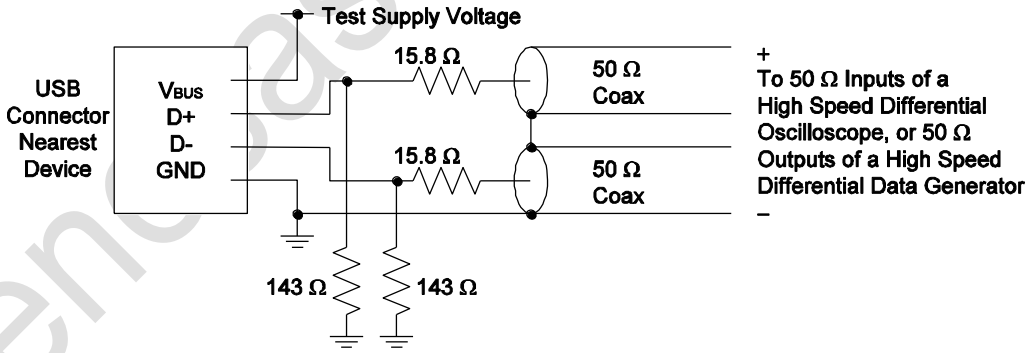


Figure3-7. Transmitter Measurement Fixtures



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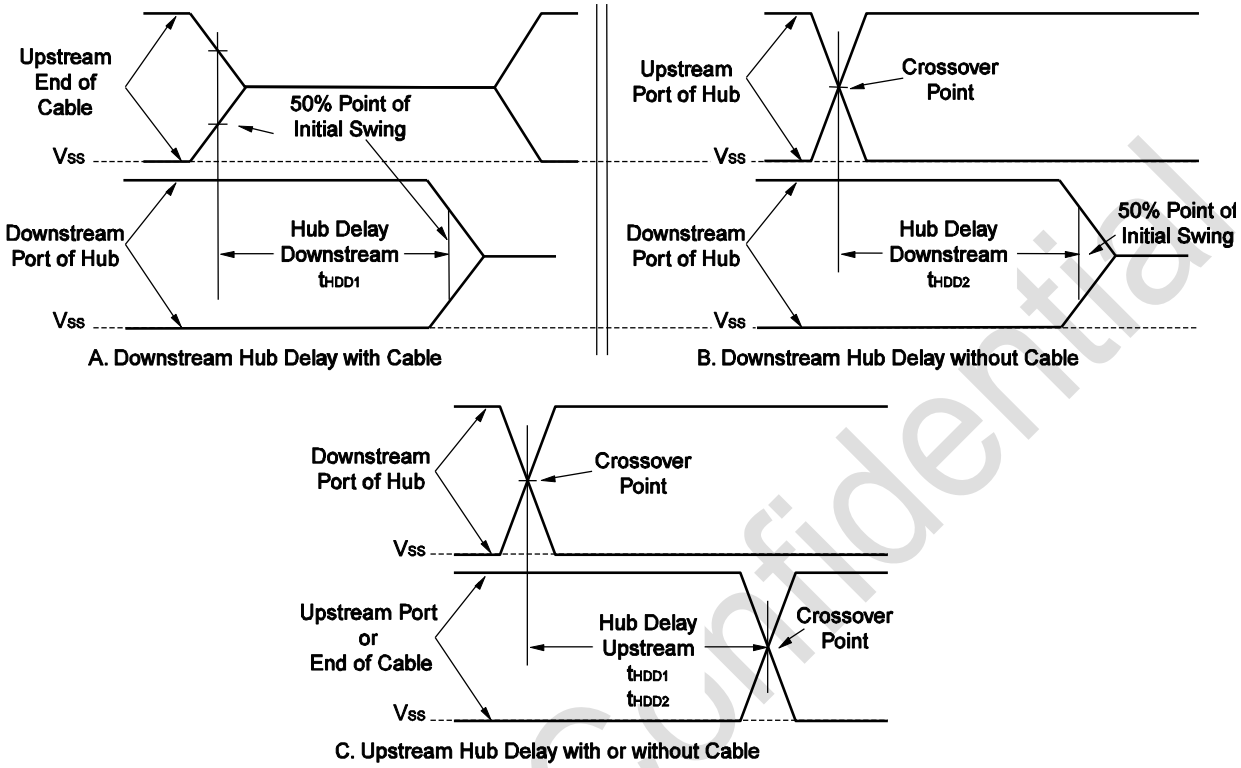
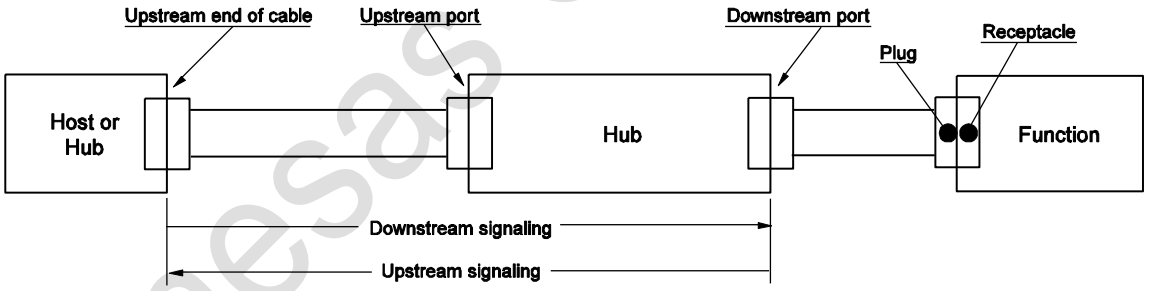
Timing Diagram

Figure3-8. Hub Differential Delay, Differential Jitter, and SOP Distortion





D. Measurement Points

Hub Differential Jitter:
$t_{HDJ1} = t_{HDDx}(J) - t_{HDDx}(K)$ or $t_{HDDx}(K) - t_{HDDx}(J)$ Consecutive Transitions
$t_{HDJ2} = t_{HDDx}(J) - t_{HDDx}(J)$ or $t_{HDDx}(K) - t_{HDDx}(K)$ Paired Transitions

Bit after SOP Width Distortion (same as data jitter for SOP and next J transition):
$t_{FSOP} = t_{HDDx}$(next J) – t_{HDDx}(SOP)

Low-speed timings are determined in the same way for:
t_{LHDD}, t_{LDHJ1}, t_{LDJH2}, t_{LUHJ1}, t_{LUJH2}, and t_{LSOP}

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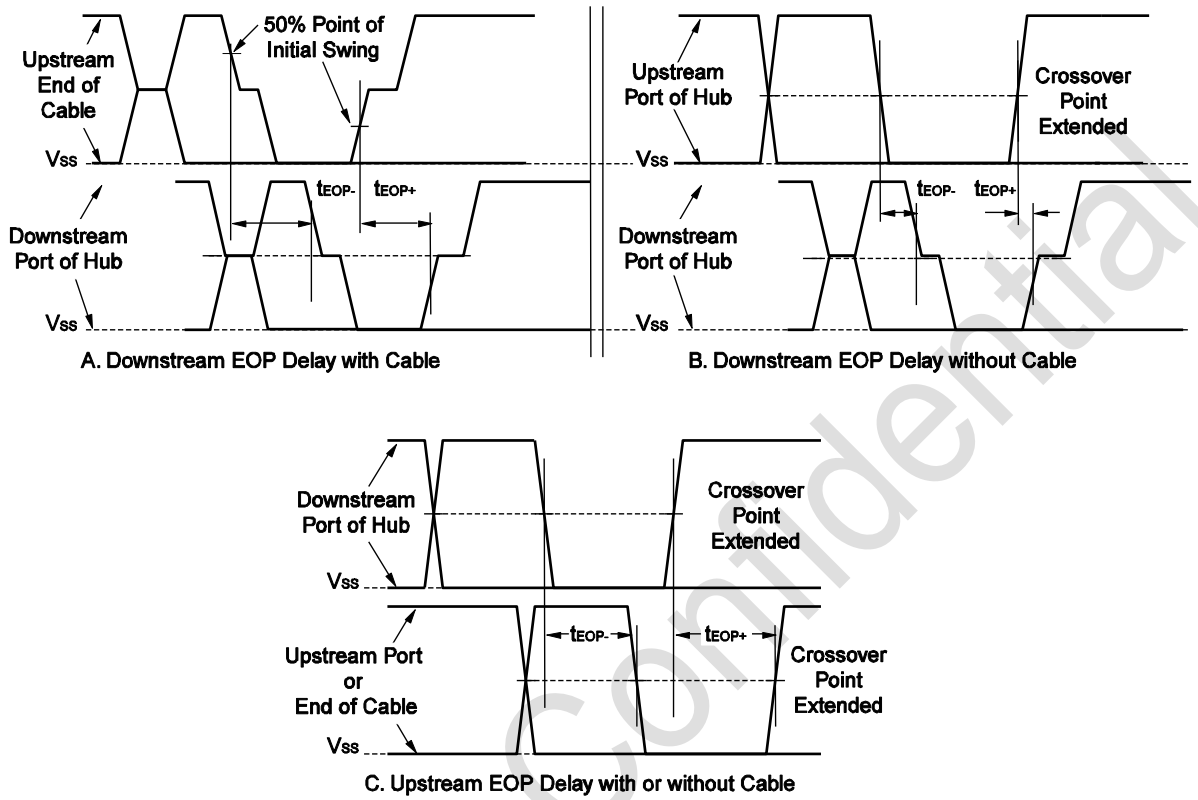
Figure 3-9. Hub EOP Delay and EOP Skew



EOP Delay:
$t_{FEOPD} = t_{EOPy} - t_{HDDx}$
(t_{EOPy} means that this equation applies to t_{EOP-} and t_{EOP+})

EOP Skew:
$t_{FHESK} = t_{EOP+} - t_{EOP-}$

Low-speed timings are determined in the same way for:
t_{LEOPD} and t_{LHESK}

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Figure3-10. USB Differential Data Jitter for Low-/full-speed

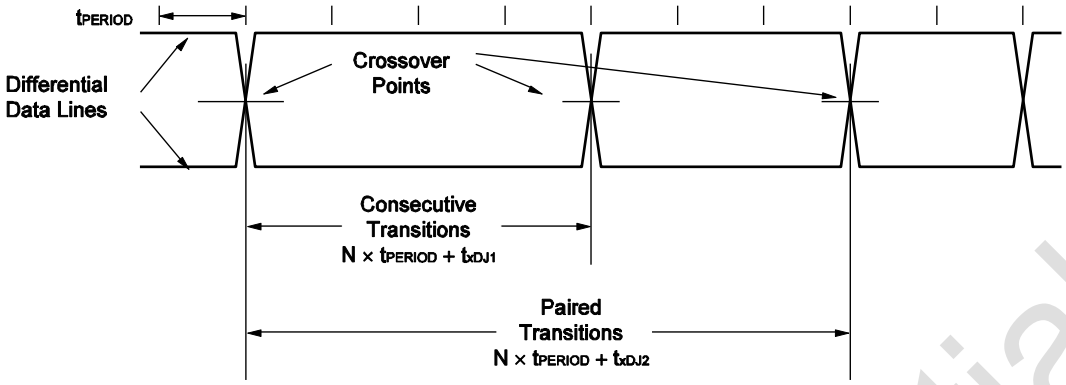

Figure3-11. USB Differential-to-EOP Transition Skew and EOP Width for Low-/full-speed

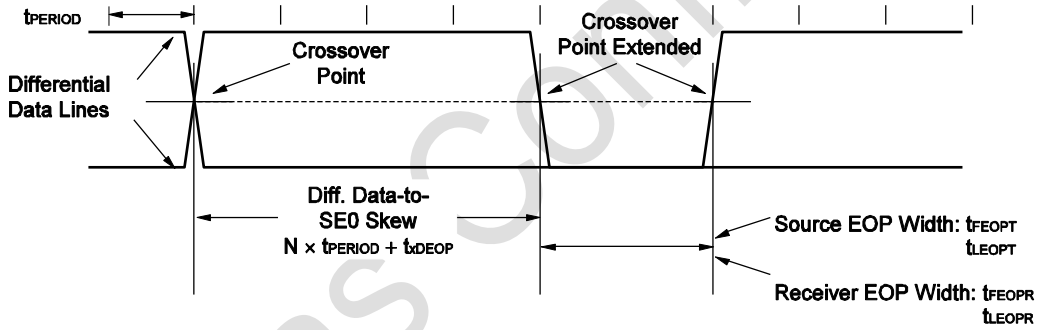

Figure3-12. USB Receiver Jitter Tolerance for Low-/full-speed

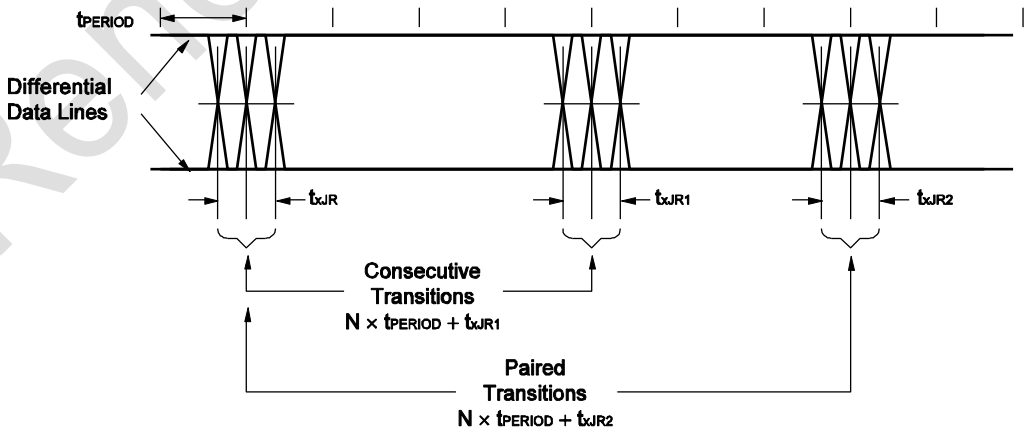

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Figure3-13. Low-/full-speed Disconnect Detection

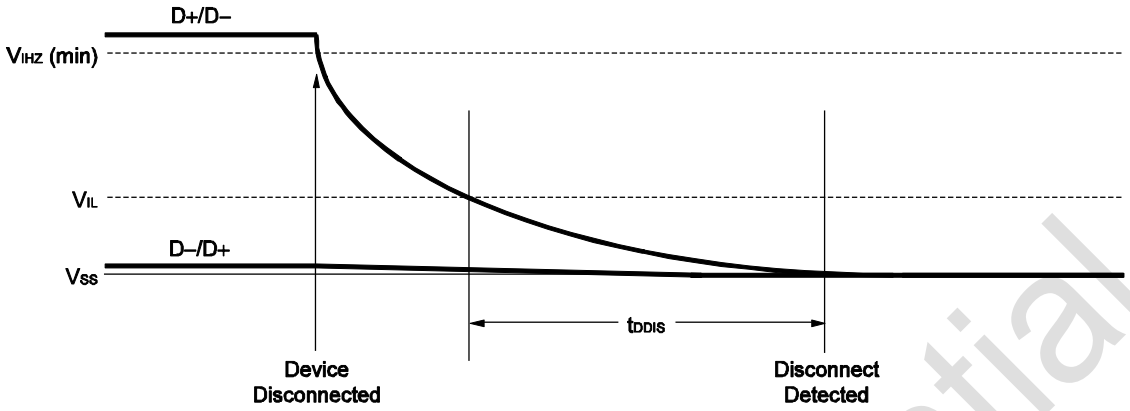


Figure3-14. Full-/high-speed Device Connect Detection

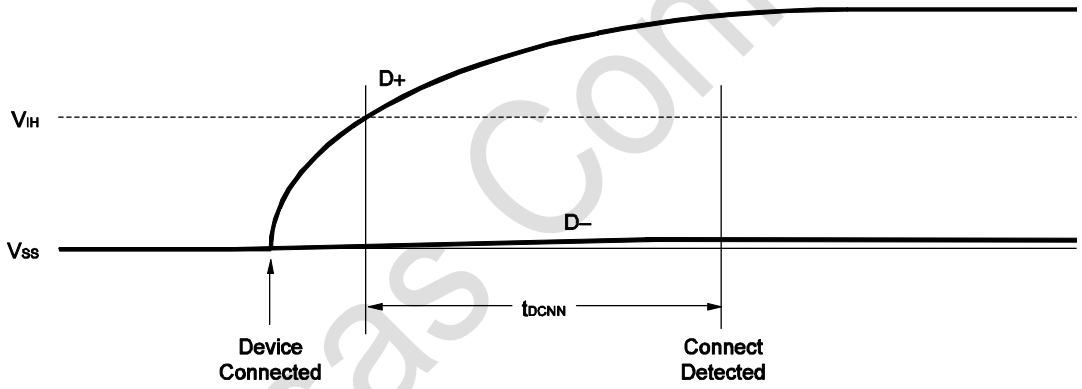
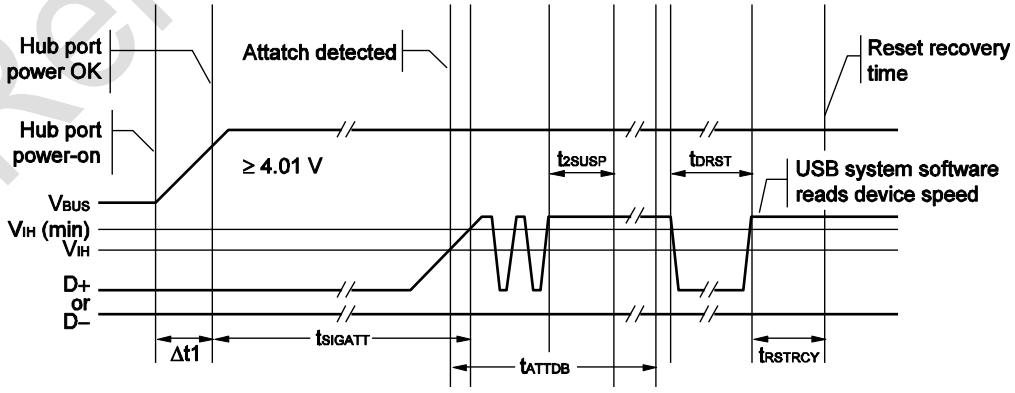


Figure3-15. Power-on and Connection Events Timing



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USB3.0 Hub Parameters

Name	Description	Min	Max	Units
tDownLinkStateChange	Time from receiving the route string of a header packet directed to a downstream port that is in a low power link state to initiating a return to U0 on the downstream link.	0	100	ns
sDataSymbolsBabble	The number of symbols in a data packet payload after the DPPSTART ordered set without and Data Packet Payload ending frame ordered set or DPPABORT ordered set that shall cause a device to detect the packet is invalid.	1030	N/A	symbols
tHubPropRemoteWakeUpstream	Time from start of remote wakeup signaling on the downstream port a hub to when the hub must propagate the remote wakeup signaling on its upstream port if the upstream port link is in U3.	0	1	ms
tHubDriveRemoteWakeDownstream	Time from receiving a SetPortFeature(PORT_LINK_STATE) U0 for a downstream port with a link in U3 to driving remote wakeup signaling on the link.	0	1000	ns
tHubPort2PortExitLat	Time from a downstream port's link initiating a U-state change to when a hub must initiate a U-state change on the upstream port's link (when required).	0	1	μs
aCurrentUnit	Unit for reporting the current draw of hub controller circuitry in the hub descriptor.		4	mA
nMaxHubPorts	Maximum number of ports on a USB 3.0 hub.		15	Ports
tTimeForResetError	If the downstream port link remains in RxDetect.active for this length of time during a warm reset, the reset is considered to have failed.	100	200	ms
tCheckSuperSpeedOnReset	Time from when a device (not a hub) detects a USB 2.0 bus reset to when the device port must enter the USPORT.Powered-On state.	0	1	ms
tUSB2SwitchDisconnect	Time from when a device (not a hub) enters USPORT.Training to when the device must disconnect on the USB 2.0 interface if the device is connected on USB 2.0.	0	1	ms
tPropagationDelayJitterLimit	Variation from the minimum time between when the last symbol of a header packet routed to a downstream port with a link in U0 is received on a hub upstream port and when the first symbol of the header packet is transmitted on the hub downstream port. ITP propagation shall meet tPropagationDelayJitterLimit for all downstream ports that transmit the ITP.	0	8	ns

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nSkipSymbolLimit	Average number of symbols between transmitted SKP ordered sets.	354	354	Symbols

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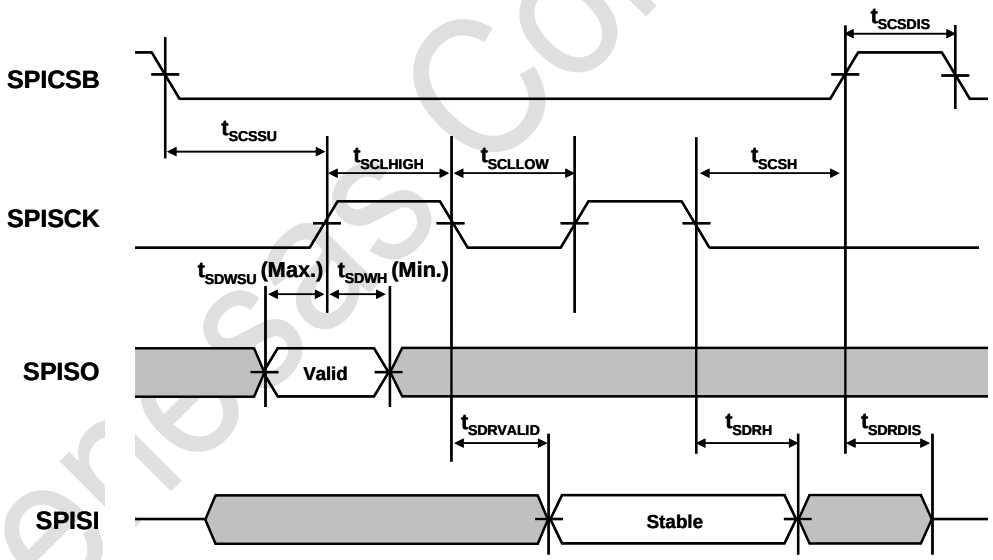
3.8.6 SPI Type Serial ROM Interface (TBD)

Table 3-14 SPI Type Serial ROM Interface Signals Timing (SPI Mode 0)

Parameter	Symbol	Min.	Max.	Units
SPISCK Clock Frequency				MHz
Clock pulses width Low	t_{SCLLOW}			ns
Clock pulses width high	$t_{SCLHIGH}$			ns
SPICSB disable time	t_{SCSDIS}			ns
SPICSB setup time	t_{SCSSU}			ns
SPICSB hold time	t_{SCSH}			ns
SPISI setup time to SPISCK rising edge	t_{SDWSU}			ns
SPISI hold time from SPISCK rising edge	t_{SDWH}			ns
SPISO validate time from SPISCK falling edge	$t_{SDRVALID}$			ns
SPISO hold time from SPISCK falling edge	t_{SDRH}			ns
SPISO disable time from SPICSB disabled	t_{SDRDIS}			ns

Figure 3-16 SPI Type Serial ROM Signal Timing



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3.9 Power Consumption (TBD)

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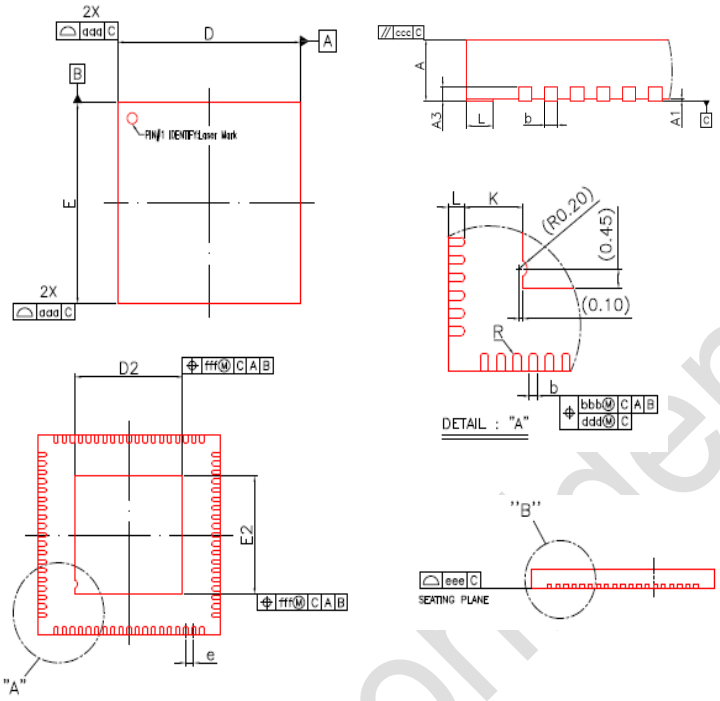
4. PACKAGE DRAWINGS

• μPD720210K8-BAF-A

76-PIN QFN (9x9)



SYMBOL	MILLIMETER		
	MIN.	TYP.	MAX.
A	- - -	- - -	0.9
A1	- - -	- - -	0.06
A3	0.20 REF		
b	0.15	0.2	0.25
D	9.00 bsc		
D2	5.15	5.3	5.45
E	9.00 bsc		
E2	5.15	5.3	5.45
L	0.3	0.4	0.5
e	0.40 bsc		
R	0.075	- - -	- - -
K	NA (0.20)	- - - -	- - - -
TOLERANCE OF FORM AND POSITION			
aaa			0.1
bbb			0.07
cccc			0.1
ddd			0.05
eee			0.08
fff			0.1

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5. RECOMMENDED SOLDERING CONDITIONS

TBD

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REVISION HISTORY	μPD720210 Preliminary Data Sheet

Rev.	Date	Description	
		Page	Summary
0.10	Sept. 30, 2011	-	First Edition issued
0.11	Oct. 31, 2011		Pin Name changed. (U2DNx → U2DMx) Fig. 1-2 Changed. (names of Pin18 and Pin19)
0.12	Feb. 21, 2012		Part Number added
0.13	Feb. 22, 2012		Part Number updated
0.14	Mar. 16, 2012		Removed Package Drawing for future update
0.15	Apr. 26, 2012	p.3, p.5, p.6, p.35	Changed Block Diagram, Pin out, 1v → 1.05v Added Package Drawing

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